Using the TPS5124EVM-001

User's Guide

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It is important to operate this EVM within the input voltage range of 0 Vdc to100 Vdc.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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High-Performance Dual Synchronous Buck Conversion Using the TPS5124

Systems Power

Contents

1 Introduction

The TPS5124 is a dual independent synchronous buck controller. Both controllers internal to the TPS5124 operate at 180° phase shift and the input ripple is partially cancelled and therefore the required input capacitance is reduced. Other features include separate soft-start circuit and standby control. See the TPS5124 data sheet (SLUS571) for detail.

2 Features

This EVM is designed to operate from 12-V bus voltage. It generates two outputs, 3.3 V at 15 A and 1.5 V at 10 A.

Table 1. TPS5124EVM−001 Performance Summary

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range		6.5	12.0	15.0	V
Operating frequency			300		kHz
Input ripple voltage (RMS)	V_{IN} = 12 V, I_{OUT1} = 15 A, I_{OUT2} = 10 A		92		mV
Channel 1					
Output current range	6.5 V ≤ V_{IN} ≤ 15 V	0	15	16	A
Line regulation	6.5 V ≤ V_{IN} ≤ 15 V I_{OUT} = 15 A		±0.1%		
Load regulation	1 A ≤ I_{OUT} ≤ 15 A V_{IN} = 12 V		±0.3%		
Load transient response voltage change	I_{OUT} rising from 0 A to 8.5 A		−160		mV_{PK}
	I_{OUT} falling from 8.5 A to 0 A		200		
Load transient response recovery time	I_{OUT} rising from 0 A to 8.5 A		80		µs
	I_{OUT} falling from 8.5 A to 0 A		120		
Loop bandwidth	I_{OUT} = 15 A		30		kHz
Phase margin	I_{OUT} = 15 A		55		°
Output ripple voltage	I_{OUT} = 15 A		33	66	mV_{PP}
Output rise time	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 15 A		2.85		ms
Full load efficiency	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 15 A		90.6%		
Channel 2					
Output current range	6.5 V ≤ V_{IN} ≤ 15 V	0	10	12	A
Line regulation	6.5 V ≤ V_{IN} ≤ 15 V		±0.1%		
Load regulation	1 A ≤ I_{OUT} ≤ 10 A V_{IN} = 12 V		±0.3%		
Load transient response voltage change	I_{OUT} rising from 0 A to 7.5 A		−120		mV_{PK}
	I_{OUT} falling from 7.5 A to 0 A		220		
Load transient response recovery time	I_{OUT} rising from 0 A to 7.5 A		40		µs
	I_{OUT} falling from 7.5 A to 0 A		80		
Loop bandwidth	I_{OUT} = 10 A		23		kHz
Phase margin	I_{OUT} = 10 A		55		°
Output ripple voltage	I_{OUT} = 10 A		15	30	mV_{PP}
Output rise time	V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 10 A		2.12		ms
Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.53 V, I_{OUT} = 10 A		85.5%		

3 Schematic

The schematic of TPS5124EVM is shown in Figure 1.

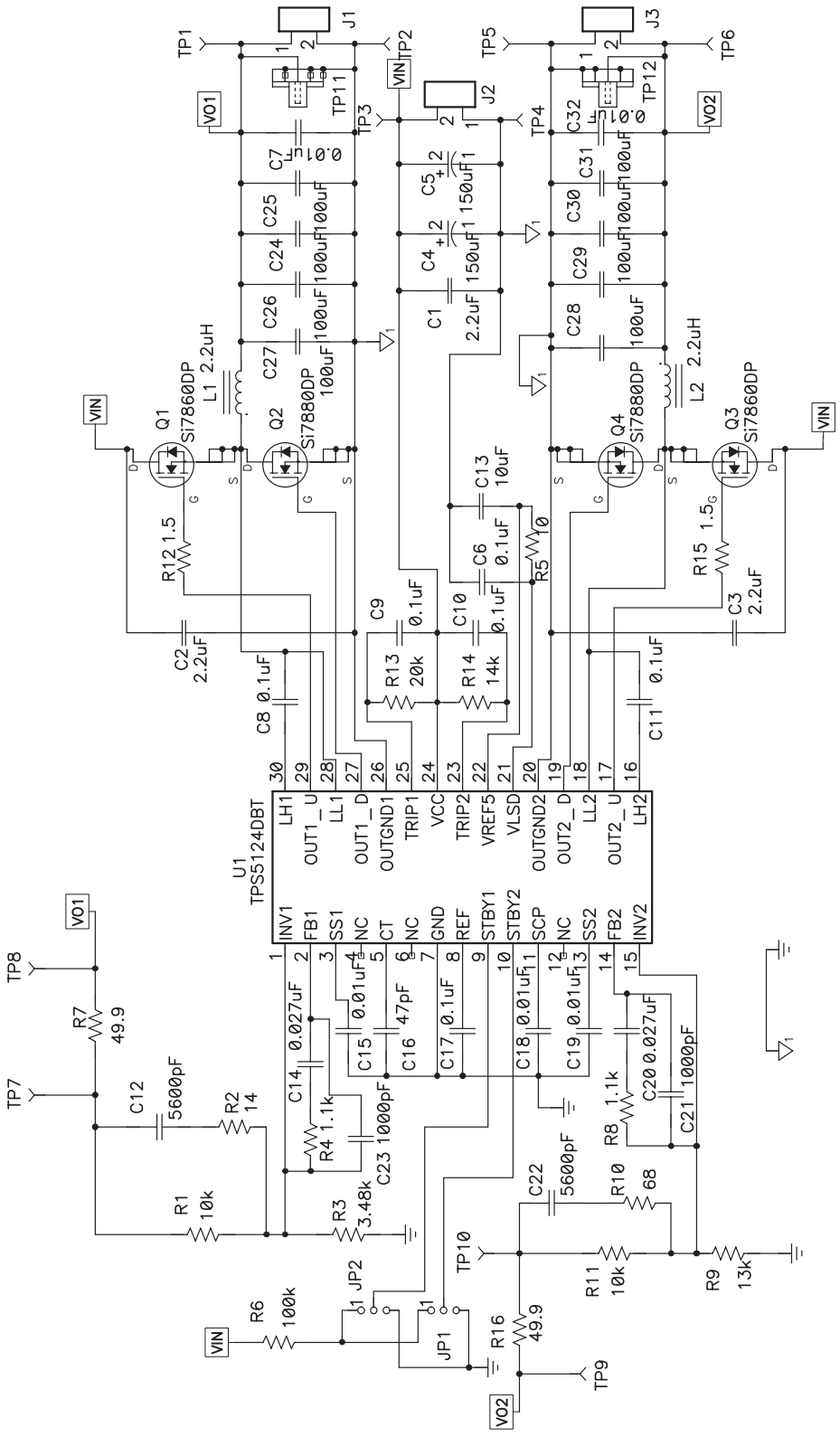

Figure 1. HPA053 TPS5124 Controller Schematic

4 Design Procedure

4.1 Frequency Setting

Many factors influence frequency selection. Higher switching frequency leads to smaller output inductor and capacitor, reducing the size of the converter. However, higher switching frequencies increase switching losses, and lower the converter's efficiency. A frequency of 300 kHz is chosen for this design for reasonable efficiency and size.

Capacitor C16, which is connected from CT (pin 5) to ground, programs the oscillator frequency. A C16 value of 47 pF yields a switching frequency of 300 kHz at 25°C.

4.2 Inductance Value

The inductance value can be calculated using equation (1).

$$L = \frac{V_{OUT}}{f\,(\text{min}) \times I_{RIPPLE}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \quad (1)$$

where

- I_{RIPPLE} is the ripple current flowing through the inductor

The ripple current affects the output voltage ripple and core losses. Based on 20% ripple current and 300 kHz, the inductance value is calculated as 2.2 µH. An off-the-shelf 2.2-µH inductor from Vishay is chosen. The part number is IHLP−5050CE−01−2R2M01. The DCR is 7 mΩ and the DCR related conduction loss is 1.6 W, which is about 3.3% of output power.

The same procedure is followed to choose the inductor for Channel 2. The same inductor is chosen.

4.3 Output Capacitors

The required output capacitance and its ESR can be calculated using equations (2) and (3).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} \quad (2)$$

$$ESR_{OUT} = \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (3)$$

With 1% output voltage ripple, the required minimum output capacitance is 54 µF and its ESR should be less than 7.7 mΩ.

From the load transient point of view, the capacitance needed for 6% overshoot can be calculated using equation (4).

$$C_{OUT} = \frac{\left(I_{OUT(max)}\right)^2 \times L}{\left(V_{OUT2}\right)^2 - \left(V_{OUT1}\right)^2} \quad (4)$$

where

- V_{OUT2} is the allowed overshoot voltage
- V_{OUT1} is the nominal operating voltage

For 6% overshoot, the required capacitance is about 370 µF. Four 100-µF, 6.3-V ceramic capacitors are used. Their ESR value is 2.0 mΩ each.

4.4 Input Capacitors

Due to the out of phase operation, the input current ripple is partially cancelled. The total RMS current in the input capacitor is calculated as follows. This assumes the total input current goes into the input capacitor to the power ground and ignores the ripple current in the inductor.

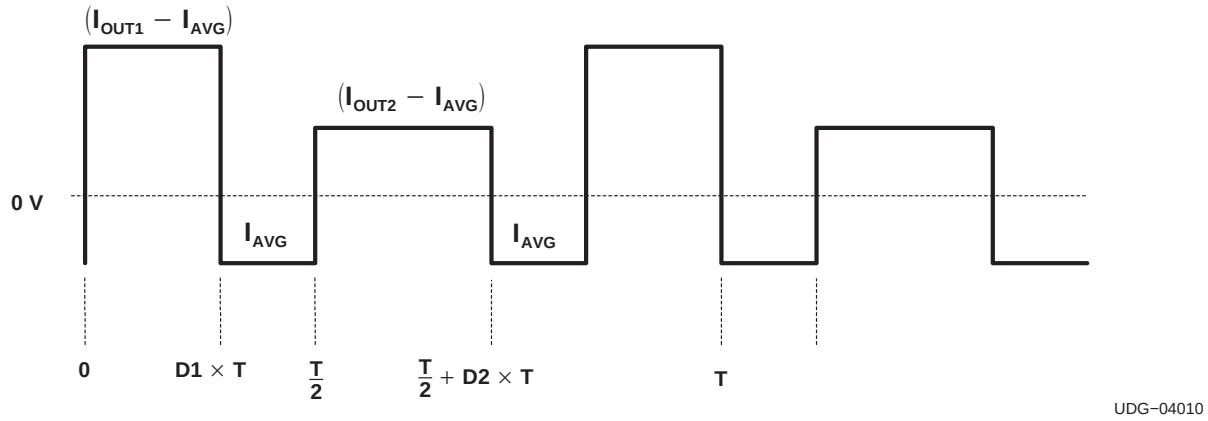

Figure 2. Case One (D1 < 0.5, D2 < 0.5)

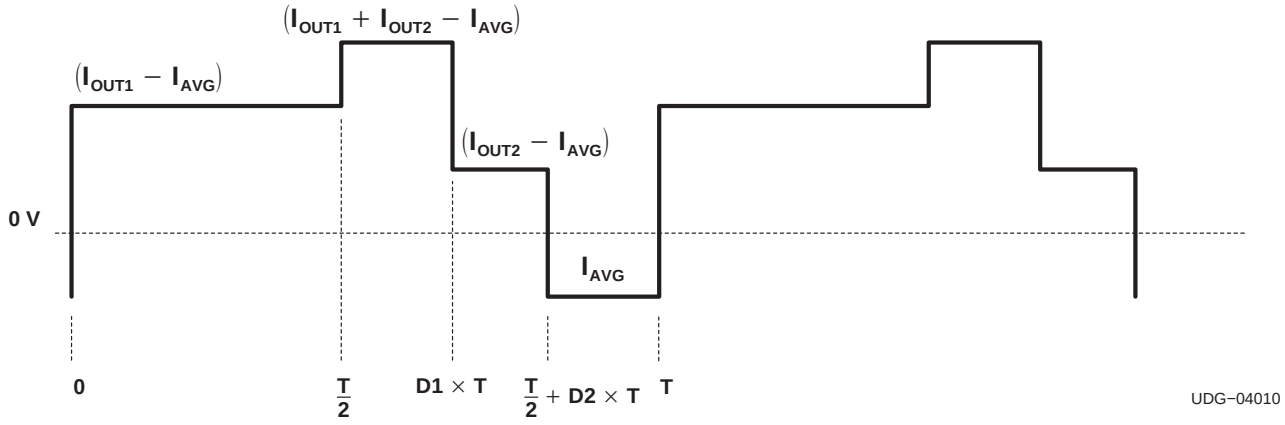

Figure 3. Case Two (D2 < 0.5 < D1)

4.4.1 Case One: D1, D2 < 0.5.

The ripple current through the input capacitor is shown in Figure 2 and can be calculated using equation (6).

$$I_{incapRMS} := \sqrt{\frac{1}{T} \times \left[\int_0^{D1 \cdot T} \left(I_{OUT1} - I_{AVG}\right)^2 dt + \int_{D1 \cdot T}^{\frac{T}{2}} \left(I_{AVG}\right)^2 dt + \int_{\frac{T}{2}}^{\frac{T}{2}+D2 \cdot T} \left(I_{OUT2} - I_{AVG}\right)^2 dt + \int_{\frac{T}{2}+D2 \cdot T}^{T} \left(I_{AVG}\right)^2 dt \right]} \quad (5)$$

$$I_{incapRMS} := \sqrt{D1 \times \left(I_{OUT1}\right)^2 + D2 \times \left(I_{OUT2}\right)^2 - \left(I_{AVG}\right)^2} \quad (6)$$

where:

I_{AVG} is the average input current.

$$I_{AVG} = I_{OUT1} \times D1 + I_{OUT2} \times D2 \quad (7)$$

4.4.2 Case Two: D2 < 0.5 < D1.

The ripple current through the input capacitor is shown in Figure 3 and can be calculated using equation (8).

$$I_{incapRMS} := \sqrt{\frac{1}{T} \times \left[\int_0^{\frac{T}{2}} \left(I_{OUT1} - I_{AVG}\right)^2 dt + \int_{\frac{T}{2}}^{D1 \cdot T} \left(I_{OUT1} + I_{OUT2} - I_{AVG}\right)^2 dt + \int_{D1 \cdot T}^{\frac{T}{2}+D2 \cdot T} \left(I_{OUT2} - I_{AVG}\right)^2 dt + \int_{\frac{T}{2}+D2 \cdot T}^{T} \left(I_{AVG}\right)^2 dt \right]} \quad (8)$$

$$I_{incapRMS} := \sqrt{D1 \times \left(I_{OUT1}\right)^2 + D2 \times \left(I_{OUT2}\right)^2 + (2 \times D1 - 1) \times I_{OUT1} \times I_{OUT2} - \left(I_{AVG}\right)^2} \quad (9)$$

This EVM meets “Case One” criteria. The maximum input ripple current is 6.7 A at V_{IN} =12 V. Two 150-µF, 20-V special polymer capacitors from Panasonic (part number is EEFWA1D151P) are used. It can handle 3.7 A of ripple current each. The ESR value of each capacitor is 26 mΩ. So the input ripple voltage is calculated using equation (10) and is approximately 88 mV_{RMS}

$$I_{RIPPLE} = I_{incapRMS} \times ESR \quad (10)$$

4.5 Compensation Design

The following compensation loop design uses Channel 1 as example, but a design for Channel 2 follows the same rules.

TPS5124 uses voltage-mode control method. A Type III compensation network, formed by R1, R2, R4, C14, C12, and C23, is used to guarantee the stability. The L-C frequency of the power stage is around 5.4 kHz and the ESR zero is at 790 KHz due to the low ESR of the ceramic capacitors. An overall crossover frequency (f_{0db}) of 30 kHz is chosen for reasonable transient response and stability. Both zeros (f_{Z1} and f_{Z2}) from the compensator are set at 2.68 kHz. The two poles (f_{P1} and f_{P2}) and are set at 150 kHz and 2 MHz. The frequency of poles and zeros are defined by the following equations.

$$f_{Z1} = \frac{1}{2\pi \times R4 \times C14} \tag{11}$$

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C12}, \quad \text{assuming } R1 \gg R2 \tag{12}$$

$$f_{P1} = \frac{1}{2\pi \times R4 \times C23} \tag{13}$$

$$f_{P2} = \frac{1}{2\pi \times R2 \times C12}, \quad \text{assuming } C14 \gg C23 \tag{14}$$

The transfer function for the compensator is calculated as:

$$A(s) = \frac{(1 + s \times C14 \times R2) \times [1 + s \times C12 \times (R1 + R2)]}{s \times R1 \times C14 \times \left[\left(1 + \frac{C23}{C14}\right) + s \times R4 \times C23\right] \times (1 + s \times R2 \times C12)} \tag{15}$$

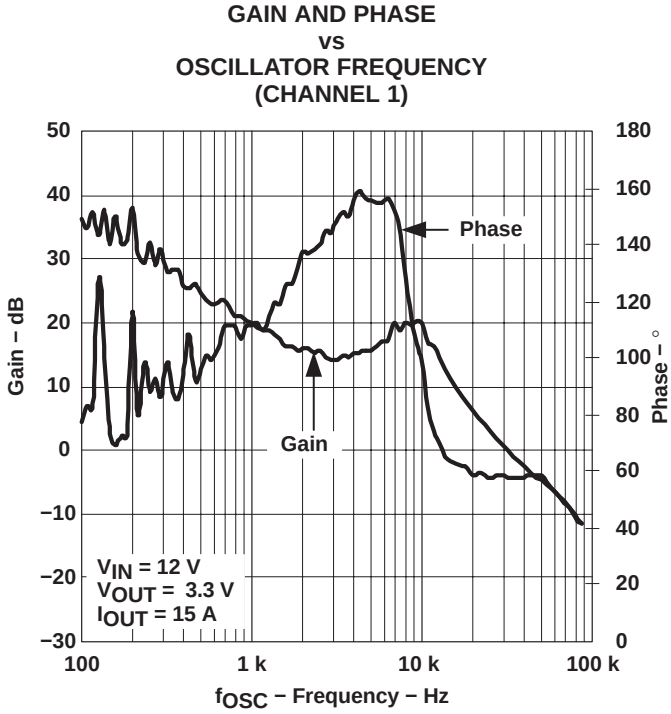

Figure 4.

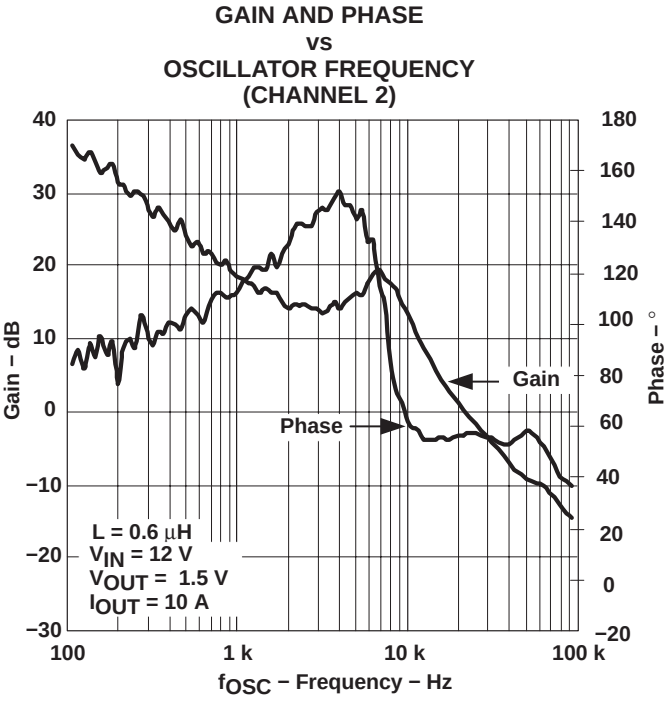

Figure 5. Channel 2

Figure 4 shows the closed loop gain and phase. For Channel 1, the overall crossover frequency is approximately 30 kHz and the phase margin is 58°. For Channel 2, the crossover frequency is approximately 23 kHz and phase margin is 55°.

4.6 Current Limiting

The current limit in TPS5124 is set using an internal current source and an external resistor (R13 and R14). The current limit protection circuit compares the drain to source voltage of the high-side and low-side drivers with respect to the set-point voltage. If the voltage exceeds the limit during high side conduction, the current limit circuit terminates the high side driver pulse. If the set point voltage is exceeded during low side conduction, the low side pulse is extended through the next cycle. Together this action has the effect of decreasing the output voltage until the under voltage protection circuit is activated and the fault latch is set and both the high-side and low-side MOSFET drivers are shut off. Equation (16) should be used for calculating the external resistor value for current protection set point.

$$R_{CL} = \frac{1.3 \times R_{DS(on)} \times \left(I_{LIM} + \frac{I_{RIPPLE}}{2} \right)}{I_{TRIP}} \quad (16)$$

where

- R_{CL} is external current limit resistor (R13 and R14)
- $R_{DS(on)}$ is the on−resistor of low side MOSFET (Q2 and Q4)
- 1.3 is the temperature coefficient of the $R_{DS(on)}$
- I_{LIM} is the required current limit
- I_{TRIP} is the internal current source with a typical value of 13 μA at 25°C

4.7 Timer Latch

The TPS5124 includes fault latch function with a user adjustable timer to latch the MOSFET drivers in case of a fault condition. When either the OVP or UVP comparator detect a fault condition, the timer starts to charge C18, the external capacitor connected to the SCP pin. The circuit is designed so that for any value of C18, the undervoltage latch time t_{UVPL} is about five times larger than the overvoltage latch time t_{OVPL}. The equations needed to calculate the required value of C18 for the desired overvoltage and undervoltage latch delay times are calculated in equations (17) or (18).

$$C18 = 1.7 \times 10^{-6} \times \frac{t_{UVPL}}{1.185} \quad (17)$$

$$C18 = 8 \times 10^{-6} \times \frac{t_{OVPL}}{1.185} \quad (18)$$

where

- C18 is the external capacitor connected to the SCP pin
- t_{UVPL} is the time from UVP detection to latch
- t_{OVPL} is the time from OVP detection to latch

For the EVM, t_{UVPL} = 7 ms and t_{OVPL} = 1.5 ms, so C18 = 0.01 μF.

If the voltage on the SCP pin reaches 1.185 V, the fault latch is set, and the MOSFET drivers are set as follows:

4.7.1 Undervoltage Protection

The under voltage comparator circuit continually monitors the voltage at the INV pin. If the voltage at that pin falls below 78% of the 0.85-V reference, the timer begins to charge C18. If the fault condition persists beyond the time t_{UVPL}, the fault latch is set and both the high-side and low-side drivers is forced OFF.

4.7.2 Short circuit Protection

The short circuit protection circuitry uses the UVP circuit to latch the MOSFET drivers. When the current limit circuit limits the output current, then the output voltage goes below the target output voltage and UVP comparator detects a fault condition as described above.

4.7.3 Overvoltage Protection

The over voltage comparator circuit continually monitors the voltage at the INV pin. If V_{INV} rises above 112% of the 0.85-V reference, the timer begins to charge C18. If the fault condition persists beyond the time t_{OVPL}, the fault latch is set and the high-side drivers are forced OFF, while the low-side drivers are forced ON.

CAUTION:

DO NOT set the SCP terminal to a voltage lower than 1.185 V while the device is timing out an OVP or UVP event. If the SCP terminal is manually set to a voltage lower than 1.185 V during this time, output overshoot may occur. The TPS5124 must be reset by grounding STBYx.

4.7.4 Disabling the Protection Function

If it is necessary to disable the protection functions of the TPS5124 for troubleshooting or other purposes, the OCP, OVP and UVP circuits may be disabled.

4.7.4.1 Disabling Overcurrent Protection (OCP)

Remove the current limit resistors R13 and R14 to disable the current limit function.

4.7.4.2 Disabling Overvoltage Protection or Undervoltate Protection (OVP, UVP)

Grounding the SCP terminal can disable OVP and UVP.

5 Test Results

5.1 Efficiency Curves

The efficiency was tested under three different operation conditions.

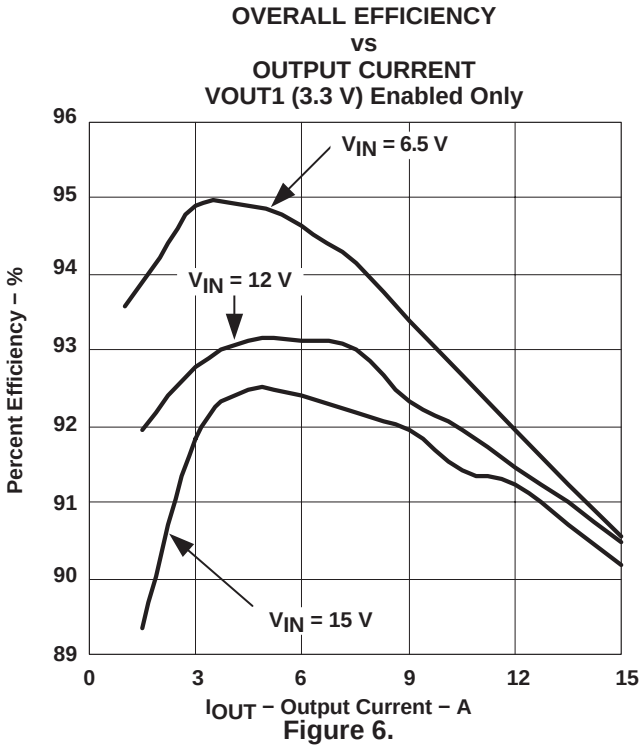

Figure 6.

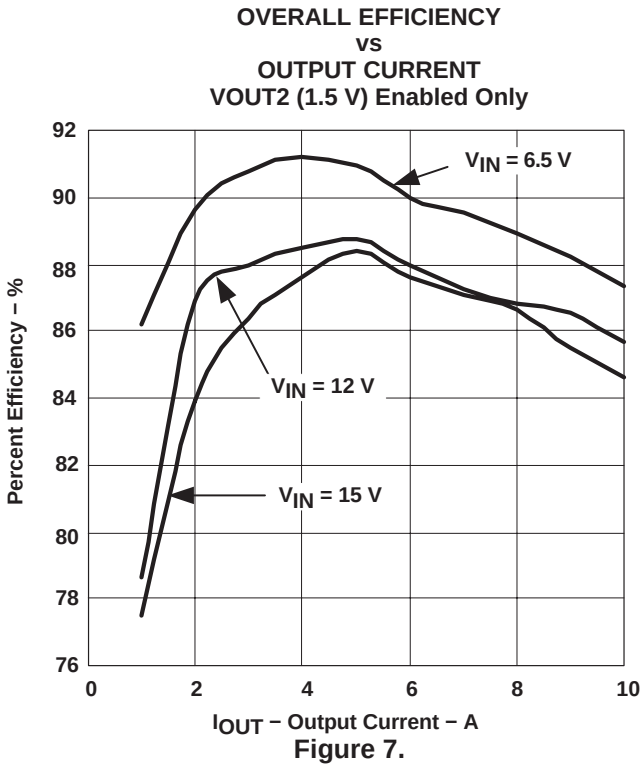

Figure 7.

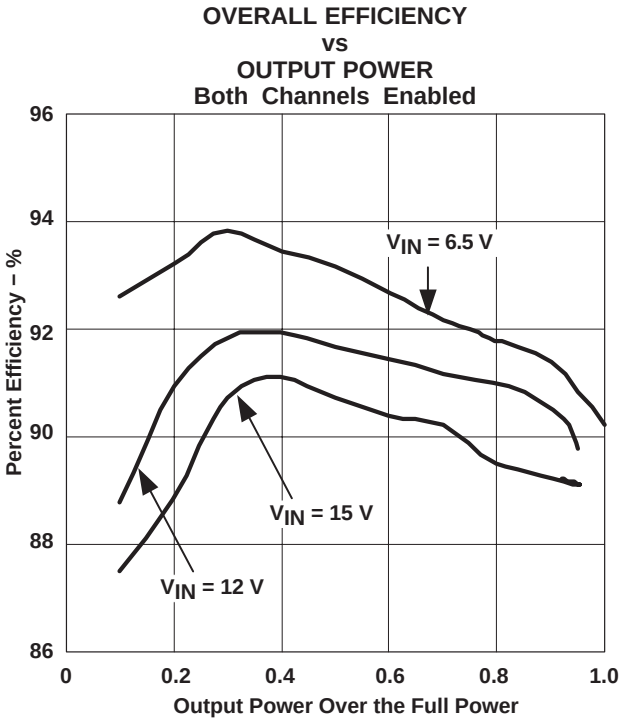

Figure 8.

5.2 Typical Operating Waveform

Typical operating waveforms taken at V_{IN} =12 V, I_{OUT1} = 15 A and I_{OUT2}=10 A is shown in Figure 9.

5.3 Start-Up Waveform

Figure 10 shows the start-up waveform taken at V_{IN} =12 V, I_{OUT1} = 15 A and I_{OUT2}=10 A. The rising time is 2.85 ms for V_{OUT1} and 2.12ms for V_{OUT2}.

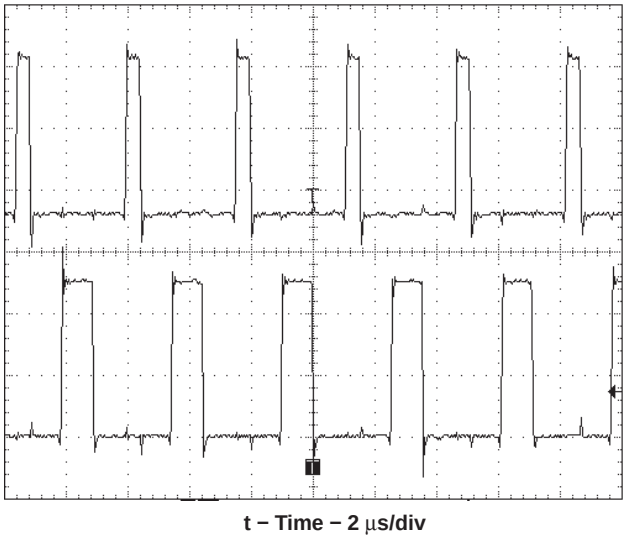

Figure 9. Switch Node Waveform

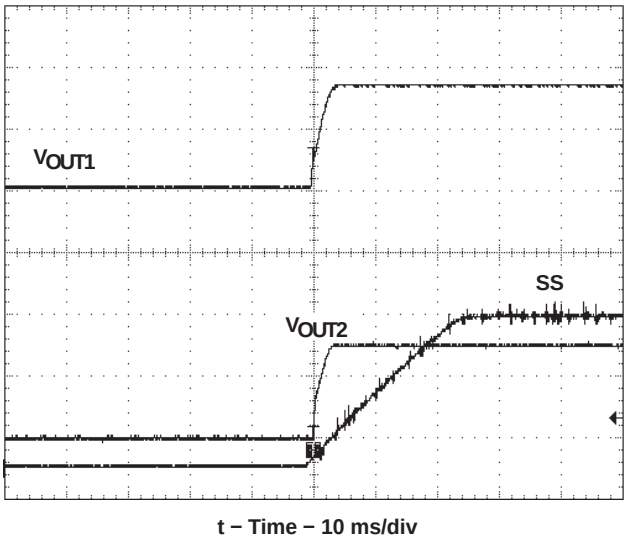

Figure 10. Start−Up Waveform

5.4 Output Ripple Voltage and Load Transient

The output ripple is about 20 mV_{P-P} at 15 A on Channel 1 (3.3 V) output and 15 mV_{P-P} at 10 A on Channel 2 output as shown in Figure 11.

Figure 12 shows the load transient response. For Channel 1 (3.3 V), when the load steps from 0 A to 8.5 A, the overshoot and undershoot voltages are about 150 mV. For Channel 2 (1.5 V), when the load steps from 0 A to 7.5 A, the overshoot voltage is approximately 220 mV and the undershoot voltage is approximately 140 mV.

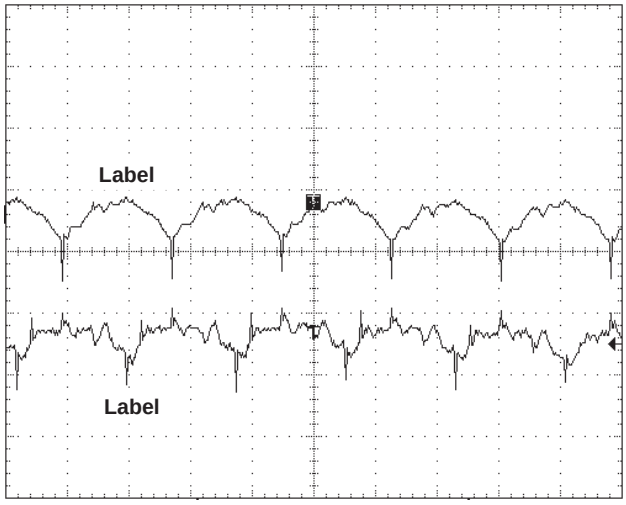

Figure 11. Output Ripple

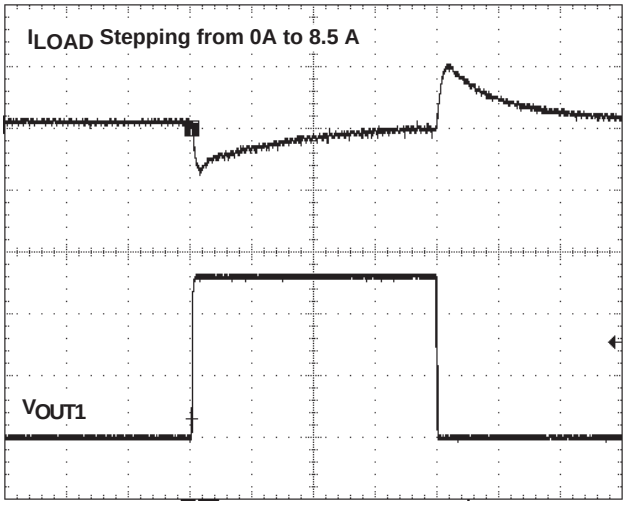

Figure 12. Load Transient Response

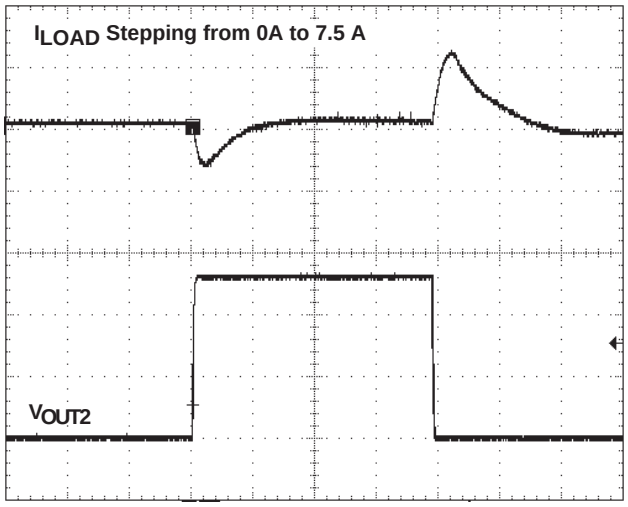

Figure 13. Load Transient Response

6 Layout Guidelines

Proper design and layout is crucial to the performance of the power supply. Here are some suggestions to the layout of TPS5124 design.

- A four−layer PCB design is recommended for designs using the TPS5124. Use at least one layer dedicated to the PWRGND plane.
- All sensitive analog components such as INV, REF, CT, GND, SCP and SOFTSTART should be reference to ANAGND.
- Ideally, all of the area directly under TPS5124 chip should also be ANAGND.
- ANAGND and PWRGND should be isolated as much as possible, with a single point connection between them

6.1 Low side MOSFET(s)

- The source of low-side MOSFET(s) should be referenced to PWRGND. Otherwise ANAGND is subject to the noise of the outputs.
- PWRGND should be placed close to the source of low-side MOSFET(s).

6.2 Connections

- Connections from the drivers to the gate of the power MOSFETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not used. In addition, external gate resistor for the high-side FET(s) will considerably reduce the noise at the LL node and improve the performance of the current limit function.
- The connection from LL to the power MOSFET(s) should be as short and wide as possible.

6.3 Bypass capacitor

- The bypass capacitor for VCC should be placed close to the TPS5124.
- The bulk storage capacitors across VCC should be placed close to the power MOSFETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side MOSFET(s) and to the source of the low-side MOSFET(s).
- For noise reduction, a 0.1-μF capacitor C_{TRIP} should be placed in parallel with the trip resistor R_{CL}.

6.4 Bootstrap capacitor

- The bootstrap capacitor CBS (connected from LH to LL) should be placed close to the TPS5124.
- LH and LL should be routed close to each other to minimize noise coupling to these traces.

- LH and LL should not be routed near the control pin area (e.g. INV, FB, REF, etc.).

6.5 Output voltage

- The output voltage sensing trace should be isolated by either ground plane.
- The output voltage sensing trace should not be placed under the inductors on the same layer.
- The feedback components should be isolated from output components, such as, MOSFETs, inductors, and output capacitors. Otherwise the feedback signal line is susceptible to output noise.
- The resistors to set up the output voltage should be referenced to ANAGND.
- The INV trace should be as short as possible.

7 PCB layout

Figures 14 through 18 shows the PCB layout.

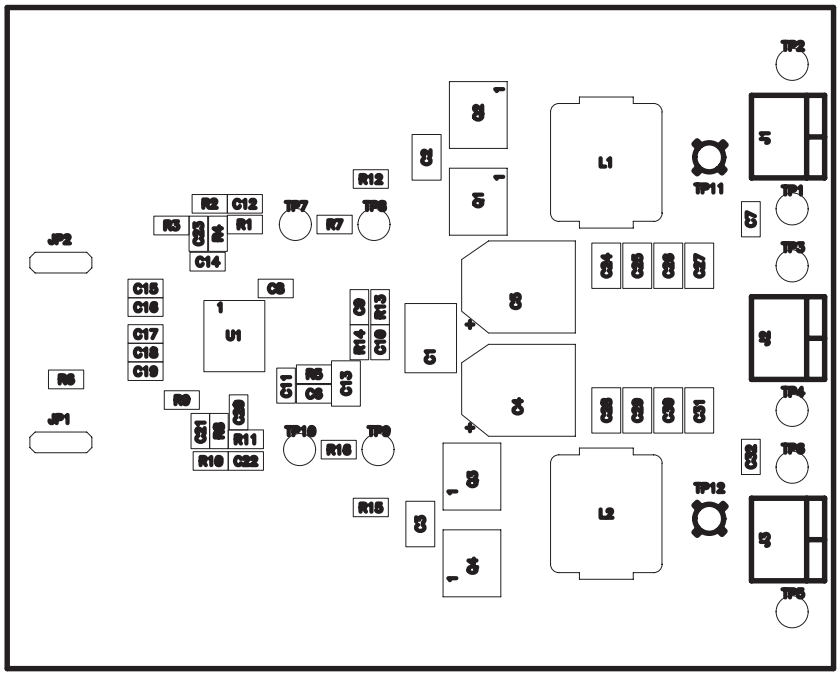

Figure 14. Top Assembly

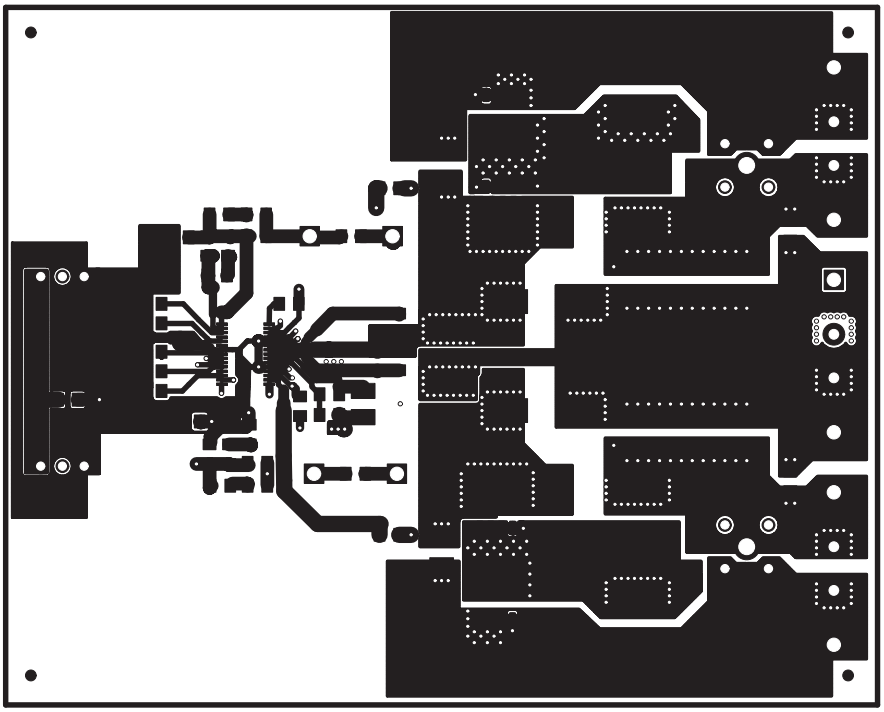

Figure 15. Top Side

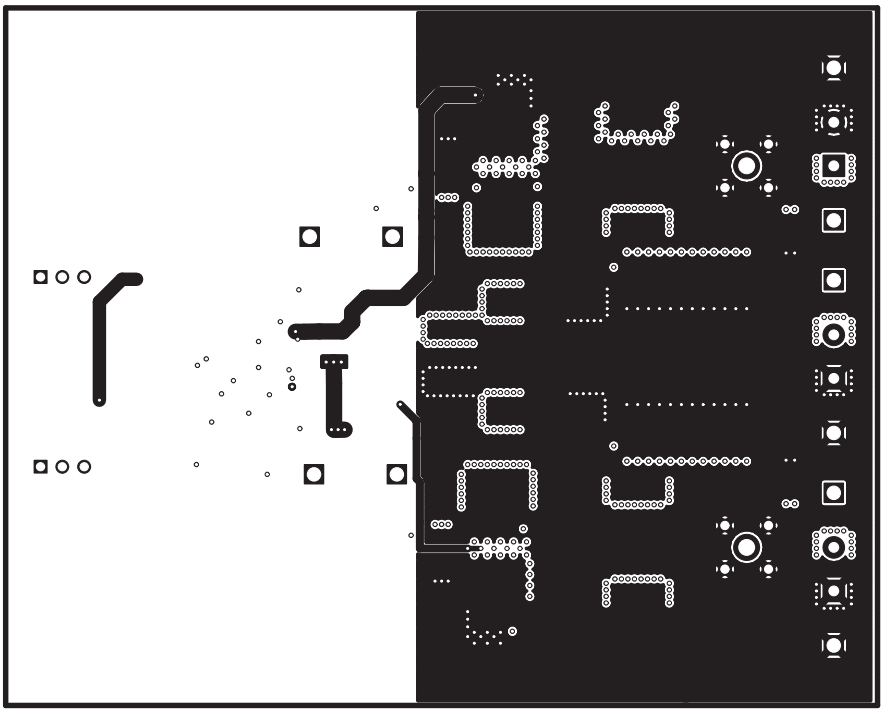

Figure 16. Internal 1

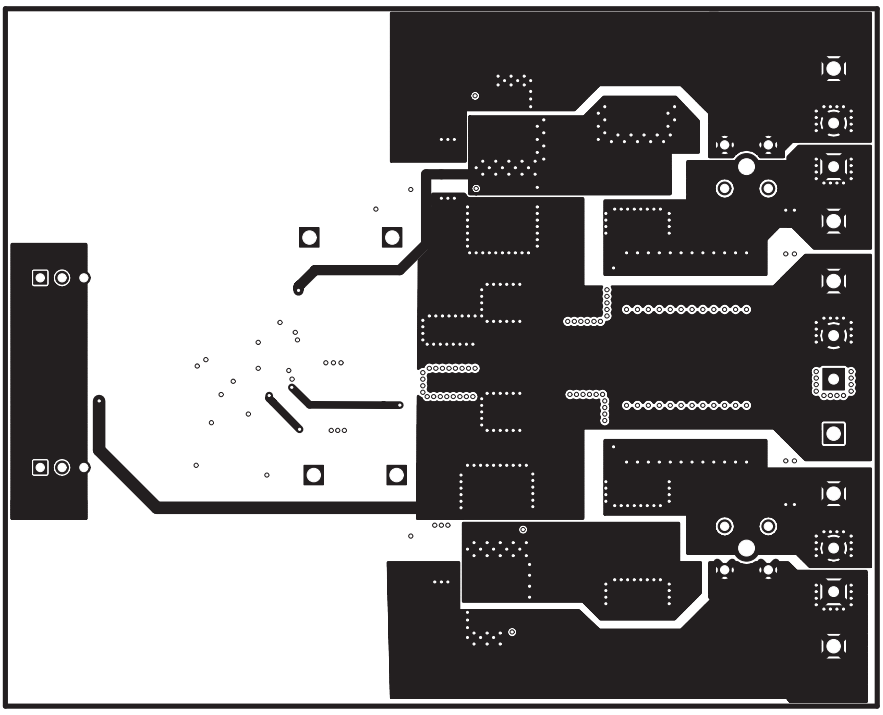

Figure 17. Internal 2

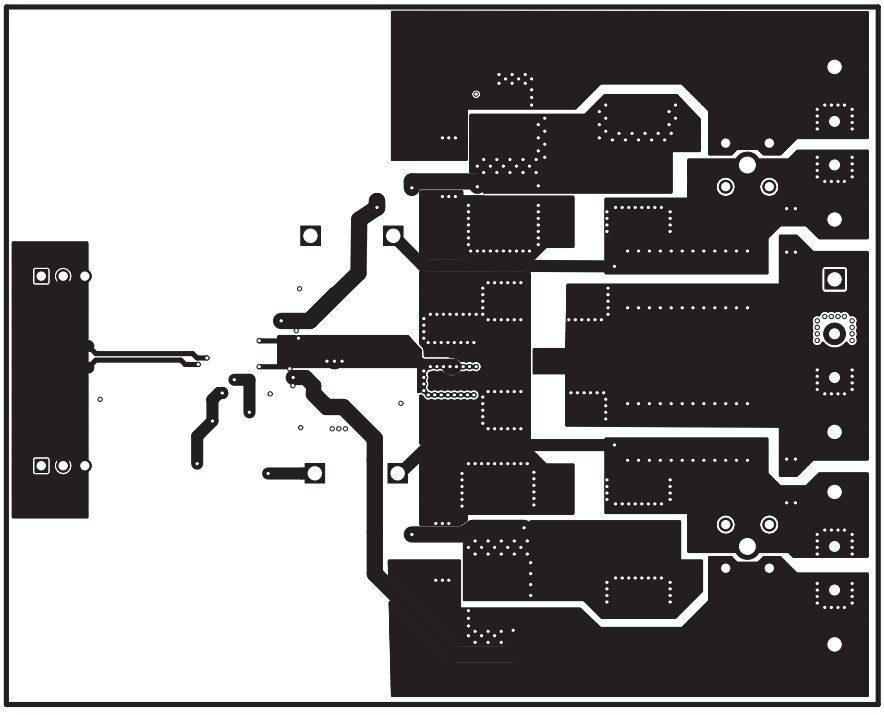

Figure 18. Bottom Side

8 List of Materials

Table 2. List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
C1,C2, C3	3	Capacitor, ceramic, 2.2 µF, 50 V, X7R, 10%	1210	Std	Std
C12, C22	2	Capacitor, ceramic, 5600 pF, 50 V, X7R, 10%	805	Std	Std
C13	1	Capacitor, ceramic, 10 µF, 10 V, X5R, 10%	1210	Murata	GRM32ER61A106KC01L
C14, C20	2	Capacitor, ceramic, 0.027 µF, 50−V, X7R, 10%	805	Std	Std
C7, C15, C18, C19, C32,	5	Capacitor, ceramic, 0.01 µF, 50−V, X7R, 10%	805	Std	Std
C16	1	Capacitor, ceramic, 47 pF, 50−V, COG, 5%	805	Std	Std
C21, C23	2	Capacitor, ceramic, 1000 pF, 50−V, COG, 5%	805	Std	Std
C24, C25, C26, C27, C28, C29, C30, C31	8	Capacitor, ceramic, 100 µF, 6.3−V, X5R	1210	TDK	C3225X5R0J107M
C4, C5	2	Capacitor, special polymer, 150 µF, 20, 20%	10.3 mm (F12)	Panasonic	EEFWA1D151P
C6,C8, C9, C10, C11, C17	6	Capacitor, ceramic, 0.1 µF, 50−V, X7R, 10%	805	Std	Std
J1, J2, J3	3	Terminal block, 2-pin, 15 A, 5.1 mm	0.40 x 0.35	OST	ED1609
JP1, JP2	2	Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN
L1, L2	2	Inductor, SMT, 2.2 µH, 20 A, 4.6 mΩ	0.51 x 0.51	Vishay−Siliconix	IHLP5050EZ−01
Q1, Q3	2	MOSFET, N-channel, 30 V, 18 A, 8.0 mΩ	PWRPAK S0−8	Vishay−Siliconix	Si7860DP
Q2, Q4	2	MOSFET, N-channel, 30 V, 29 A, 3 mΩ,	PWRPAK S0−8	Vishay−Siliconix	Si7880DP
R1, R11	2	Resistor, chip, 10.0 kΩ, 1/10−W, 1%	805	Std	Std
R10	1	Resistor, chip, 68.1 Ω, 1/10−W, 1%	805	Std	Std
R5	1	Resistor, chip, 10.0 Ω, 1/10−W, 1%	805	Std	Std
R12, R15	2	Resistor, chip, 1.5 Ω, 1/10−W, 1%	805	Std	Std
R13	1	Resistor, chip, 20.0 kΩ, 1/10−W, 1%	805	Std	Std
R14	1	Resistor, chip, 14.0 kΩ, 1/10−W, 1%	805	Std	Std
R16, R7	2	Resistor, chip, 49.9 Ω, 1/10−W, 1%	805	Std	Std
R2	1	Resistor, chip, 14 Ω, 1/10−W, 1%	805	Std	Std
R3	1	Resistor, chip, 3.48 kΩ, 1/10−W, 1%	805	Std	Std
R4, R8	2	Resistor, chip, 1.10 kΩ, 1/10−W, 1%	805	Std	Std
R6	1	Resistor, chip, 100 kΩ, 1/10−W, 1%	805	Std	Std
R9	1	Resistor, chip, 13.0 kΩ, 1/10−W, 1%	805	Std	Std
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10	Test point, 0.062 hole	0.25	Keystone	5012
TP11, TP12	2	Adaptor, 3.5 mm probe clip (or 131−5031−00)	0.2	Tektronix	131−4244−00
U1	1	IC, dual-channel synchronous step-down PWM controller	DBT30	TI	TPS5124DBT
	1	PCB, 4 In x 3.2 In x .062 In		Any	HPA053

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